LIN BAI

Ph.D in Electrical and Computer Engineering

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EXPERIENCE

Staff Architect
Black Sesame Technologies Inc.
Jul 2023 – Now | San Jose, USA

Senior Architect
Black Sesame Technologies Inc.
Jun 2022 – Jul 2023 | San Jose, USA

Architect - AI Computing
Black Sesame Technologies Inc.
Dec 2021 – Jun 2022 | San Jose, USA

- **Neural Network Accelerator Modeling:**
  (a) Build performance model & functional model for next generation NPU;
  (b) Explore design space for NPU novel architecture.
- **Implementation of Performance Monitor Tool:**
  (a) Check the performance model, plot the results in graphical way;
  (b) Analyze the deep learning DAG & supply performance improve suggestions for toolchain.

Research Assistant
Worcester Polytechnic Institute
Aug 2017 – Nov 2021 | Worcester, USA

- **Implementation of CNN accelerator on FPGA:**
  (a) A line buffer based SIMD CNN accelerator; (b) Design rules for above accelerator for efficient computation.
- **Design of hardware-friendly CNN:**
  (a) RoadNet-RT : for road segmentation task, with 92.55% accuracy on KITTI dataset, 111 frames per second in average; (b) DepthNet: for LiDAR depth completion task, saving 99% weights with 2.3% sacrifice in accuracy.

Technical Intern
The MathWorks, Inc.
May – Aug 2018 – 2020 | Natick, USA

- **Implementation of ACF vehicle detector on FPGA:**
  (a) 10 feature channels: LUV, softbin HoG, gradient magnitude; (b) 12-layer image pyramid; (c) High performance boosted decision tree with 3-stage memory hierarchy.
- **Implementation of image stabilization & stitching on FPGA:**
  (a) Pipelined structure for feature detection and feature matching; (b) Supporting up to 1024 features ; (c) Oriented FAST feature detector, BRIEF feature descriptor and RANSAC aligner.
- **Design of image resizing on FPGA :**
  A general structure supporting bi-linear, bi-cubic, and lanczos-2 interpolation algorithms.

FPGA Development Engineer
nanoTRONIC GmbH
Nov 2012 – Jul 2017 | Lyss, Switzerland

- **Design of FPGA based speed detection system for high-speed trains:**
  (a) Quadrature encoder speed detector; (b) Safety mechanism applied.
- **Design of FPGA based step motor controller for space application:**
  (a) 8 micro-step motor controller; (b) PLB to APB converter.
- **Design of a testing system for E-Bike communication module:**
  (a) Linux C programming on RaspberryPI; (b) Telit Module control using UART AT command, including GSM & GPRS checking, SMS sending, GPS checking; (c) MySQL system for results storage.

EDUCATION

Doctor of Philosophy
Worcester Polytechnic Institute, USA
Aug 2017 – Nov 2021
Thesis: Autonomous Driving Perception System on FPGA

Master of Science - Electronic Technique
ETH Zürich, Switzerland
Sep 2009 – Aug 2012
Thesis: Compressed Sensing Reconstruction on FPGA

Bachelor of Engineering - Integrated Circuits Design
University of Electronic Science and Technology of China, China
Sep 2005 – Jul 2009
Thesis: AMBA Bus based SoC Verification System

RESEARCH AREA

Deep Learning | Computer Vision | FPGA | Autonomous Driving

SKILLS

Programming Languages:
C++ | VHDL | VerilogHDL | SystemVerilog | Python

Frameworks:
Keras | PyTorch | ONNX | OpenCV

Developer Tools:
Vivado | ModelSim | Synplify Pro | Git | Docker | PyCharm

FPGA:
Xilinx Virtex-series & UltraScale MPSoC | Actel Radiation-Tolerant ProASIC3

LANGUAGES

Mandarin
English
German

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SELECTED PUBLICATIONS

[1] Bai, L., Zhao, Y. and Huang, X., **Enabling 3D Object Detection with a Low-Resolution LiDAR**, *IEEE Embedded Systems Letters*, Vol. 14, Iss. 4, 2022

[2] Bai, L., Zhao, Y., Zhang X. and Huang, X., **A Near Sensor Edge Computing System for Point Cloud Semantic Segmentation**, *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, Austin TX, United States

[3] Zhao, Y., Bai, L., Zhang Z. and Huang, X., **FIDNet: LiDAR Point Cloud Semantic Segmentation with Fully Interpolation Decoding**, *2021 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS)*, Prague, Czech Republic

[4] Zhao, Y., Bai, L., Zhang Z. and Huang, X., **A Surface Geometry Model for LiDAR Depth Completion**, *IEEE Robotics and Automation Letters (RA-L)*, Vol. 6, No. 3, 2021

[5] Bai, L., Lyu, Y. and Huang, X., **RoadNet-RT: High Throughput CNN Architecture and SoC Design for Real-Time Road Segmentation**, *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, Vol. 68, Iss. 2, 2021

[6] Bai, L., Zhao, Y. Elhousni, M. and Huang, X., **DepthNet: Real-Time LiDAR Point Cloud Depth Completion for Autonomous Vehicles**, *IEEE Access*, Vol. 8, 2020

[7] Bai, L., Lyu, Y. and Huang, X., **PointNet on FPGA for Real-Time Lidar Point Cloud Processing**, *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain

[8] Bai, L., Lyu, Y. and Huang, X., **A Unified Hardware Architecture for Convolutions and Deconvolutions in CNN**, *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain

[9] Lyu, Y., Bai, L. and Huang, X., **Road Segmentation using CNN and Distributed LSTM**, *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan

[10] Lyu, Y., Bai, L. and Huang, X., **ChipNet: Real-Time LiDAR Processing for Drivable Region Segmentation on an FPGA**, *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, Vol. 66, Iss. 5, 2018

[11] Bai, L., Zhao, Y. and Huang, X., **A CNN accelerator on FPGA using depthwise separable convolution**, *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, Vol. 65, Iss. 10, 2018

[12] Lyu, Y., Bai, L. and Huang, X., **Real-Time Road Segmentation Using LiDAR Data Processing on an FPGA**, *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy

[13] Bai, L., Maechler, P., Muehlberghuber, M. and Kaeslin, H., **High-speed compressed sensing reconstruction on FPGA using OMP and AMP**, *2012 IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Seville, Spain

GALLERY

NPU	-	Neural Processing Unit
DAG	-	Directed Acyclic Graph
CNN	-	Convolutional Neural Network
ACF	-	Aggregate Channel Features
HoG	-	Histogram of Oriented Gradient
FAST	-	Features from Accelerated Segment Test
BRIEF	-	Binary Robust Independent Elementary Features
RANSAC	-	RANdom SAmple Consensus
HLS	-	High-Level Synthesis